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| Document Name | | | | | | | | | | | | | | | | | | Document Number  00.06.01.404 | | | | | | | |
| Ford FPD LINK System Level Design Verification Checklist | | | | | | | | | | | | | | | | | |  | | | | | | | |
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| DATE | | |  | | Ver | REVISIONS | | | | | | | | | | | | |  | |  | REFERENCE | | | |
| 6/22/2018 | | |  | | AA | Initial Release | | | | | | | | | | | | |  | |  |  | | | |
| 3/21/2019 | | |  | | AB | Added requirement 3.1.2.2, removed reference to only FPD LINK III | | | | | | | | | | | | |  | |  | MODIFIED BY | | | |
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|  | | |  | |  |  | | | | | | | | | | | | |  | |  | Jim Lawlis (jlawlis@ford.com) | | | |
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# INTRODUCTION

## 1.1 Purpose

This System level document may be used to evaluate and/or certify the conformance of Ford FPD LINK vehicle networks.

Any network implementation that passes all checklist entries specified herein shall be considered “production ready”.

## 1.2 Scope

This document is a checklist that will help ensure modules incorporating an FPD LINK adhere to the Ford FPD LINK requirements.

## 1.3 Use of this document

This document provides a formal checklist to evaluate the integrity of Ford FPD LINK based vehicle system networks. Systems and subsystem integrators must perform the tests within this document as deemed within the program specific "Statement Of Work”. The tests within may be applied to any system implementation that has been designed in accordance to the Ford FPD LINK specifications identified in section 1.4 of this document. The individual test cases contained in this document may be performed in any sequence, subset, or performed repetitively, for the purposes of troubleshooting and/or evaluation. For vehicle program "Engineering Sign-Off Certification" however, all tests must be performed sequentially, in full, and have a formal TDR completed and provided to their respective Ford Mux Applications Engineering Authority. In addition, all delineations and options within this document must be identified and adhered to

## 1.4 Ford Documentation References

The requirements of the documents listed in the following table, form a part of this System Review. The revision levels shown in the table were the latest at the time this Functional Specification was written. In the event of a conflict between the requirements of this specification and these documents, the requirements of the documents in the table shall have precedence.

| **Rev Level** | **Requirement Document Name (ie, SDS/ARL requirements, Deviations, Engineering Specifications)** |
| --- | --- |
| 1 | FPD LINK Physical Layer Specification 00.06.03.004 |
| 2 | Netcom Physical Layer Approved Components 00.06.03.002 |
| 3 | Feature – I2C over LVDS Communication Protocol [VDOC038838] |
| 4 | Texas Instruments Data sheets and user guides |
| 5 | FPD Link Physical Layer Design Verification Checklist 00.06.03.401 |
| 6 | FPD Link Implementation Specification 00.06.01.004 |
| 7 | TI datasheets1 |
| 8 | FPD LINK Cable/Connector Assembly Specification 00.06.01.005 |
| 9 | FPD LINK Implementation Review Design Verification Checklist 00.06.01.405 |

Table (1)

## 1.5 Definitions/Abbreviations

### 1.5.1 General Definitions

|  |  |
| --- | --- |
| Back Channel | Low speed data channel over which command and control data is sent |
| Bus | A bus is a collection of one or more wires connecting two or more nodes. Each electronic device (in this case: Host ECU, Master Node or Slave Node) is equipped with a specific, standardised electronic interface in order to guarantee compatibility between exchanged binary items of information |
| Deserializer | The deserializer converts FPD LINK frames raw into video/display data |
| Display Processor | This is video data sink typically on the head unit or cluster or display module. It is connected to an FPD LINK Deserializer via I2C and high speed data lines. |
| Forward Channel | High speed data channel over which raw/uncompressed video data is sent |
| Host ECU | Electronic control unit that communicates on the CAN Network that uses FPD LINK to send and receive data to peripheral devices |
| Local Node | Local Node is attached to the main system processor and is responsible configuration and PowerModing of the bus |
| Multiplex | To interleave or simultaneously transmit two or more messages/signals or sets of data on a single channel. |
| Network | A set of electronic and cabling devices facilitating the multidirectional exchange of information between two or more nodes on one or more busses. |
| Remote Node | Remote Node is attached to the Local node via FPD LINK and it receives it’s configuration and Powermoding from the local node over FPD LINK |
| Sensor | This is a data source like camera imager, lidar sensor etc. It is connected to an FPD LINK Serializer via I2C and high speed data lines. The sensor can be configured from FPD LINK from the back channel data. |
| Serializer | The serializer converts raw video/display data into FPD LINK frames and sends this over the data line at high bit rates |

|  |  |
| --- | --- |
| Back Channel3 | Low speed data channel over which command and control data is sent |
| Bus | A bus is a collection of one or more wires connecting two or more nodes. Each electronic device (in this case: Host ECU, Master Node or Slave Node) is equipped with a specific, standardised electronic interface in order to guarantee compatibility between exchanged binary items of information |
| Deserializer | The deserializer converts FPD LINK frames raw into video/display data |
| Display Processor | This is video data sink typically on the head unit or cluster or display module. It is connected to an FPD LINK Deserializer via I2C and high speed data lines. |
| Forward Channel | High speed data channel over which raw/uncompressed video data is sent |
| Host ECU | Electronic control unit that communicates on the CAN Network that uses FPD LINK to send and receive data to peripheral devices |
| Local Node | Local Node is attached to the main system processor and is responsible configuration and PowerModing of the bus |
| Multiplex | To interleave or simultaneously transmit two or more messages/signals or sets of data on a single channel. |
| Network | A set of electronic and cabling devices facilitating the multidirectional exchange of information between two or more nodes on one or more busses. |
| Remote Node | Remote Node is attached to the Local node via FPD LINK and it receives it’s configuration and Powermoding from the local node over FPD LINK |
| Sensor | This is a data source like camera imager, lidar sensor etc. It is connected to an FPD LINK Serializer via I2C and high speed data lines. The sensor can be configured from FPD LINK from the back channel data. |
| Serializer | The serializer converts raw video/display data into FPD LINK frames and sends this over the data line at high bit rates |
| Pixel Clock | Product of image resolution frame rate colour depth and blanking interval |
| REF Clock | Driving FPD link when operating in sync mode |
| CSI-2 clock | Determines CSI data rate per lane |
| Ext clock mode | Clock driving serializer independent of deserializer clock |
| DVP clock | Special case of external clock for backward compatibility |
| Sync mode | Using single REF clock to drive both serializer and deserializer |
| CMLOUT | FPD link without backchannel used in dasy chain |

Table (2) Requirement Documents

### 1.5.2 Abbreviations used in this document

# 

|  |  |
| --- | --- |
| BCC | Bi-Directional Control Channel |
| DID | Diagnostic Identifiers |
| DTC | Diagnostic Trouble Code |
| ECU | Electronic Control Unit |
| EMC | Electromagnetic Compatibility |
| FMC | Ford Motor Company |
| FPD LINK | Flat Panel Display (FPD) Link (TI Devices Trademark) |
| FPS | Frames Per Second |
| ISO | International Standards Organisation |
| LVDS | Low Voltage Differential Signalling |
| PCB | Printed Circuit Board |
| PDB | Power Down Mode Pin |
| POC | Power Over Coax |
| PoDL | Power over Data Line (same as in POC) |
| SERDES | Serializer-Deserializer |
| TI | Texas Instruments |
| STP | Shielded Twisted Pair |
| CMLOUT | Current mode logic output |

Table (3) Abbreviations

# Design Verification Checklist

## 2.1 FPD LINK System Level Conformance Tests

**Complete Hardware Checklist, Cable/Connector DV, Compatabiity tests prior to reviewing this document**

All FPD LINK Nodes must demonstrate conformance to the checklist items defined in the table below:

|  |  |  |
| --- | --- | --- |
| **FPD LINK checklist items** | **Checklist items Evidence** | **Pass/ Fail/ Comments** |
| **Data Transmission Speed**  DL\_FPD LINK\_REQ\_\_3.1.1.1  DL\_FPD LINK\_REQ\_\_3.1.2.1  DL\_FPD LINK\_REQ\_\_3.1.2.2  DL\_FPD LINK\_REQ\_\_3.1.3.1  DL\_FPD LINK\_REQ\_\_3.1.4.1  What is the speed of the SerDes system  what is the maximum achievable bit rate of each SerDes  What are the supported formats  Confirm the locate node and remote node configured settings matches  Confirm the use of appropriate cable/connectors assemblies for the corresponding channel frequency range for forward and back channel. |  |  |
| **Common FPD LINK Network Wakeup Source**  DL\_FPD LINK\_REQ\_\_3.2.3.1  How does the FPD LINK network wakes up ?  How does the FPD LINK network receives vehicle power modes?  Confirm how is the remote node powered-up? |  |  |
| **Network Video Master Clock**  DL\_FPD LINK \_REQ\_\_3.3.1.4  Confirm the Video Master Clock supplied to the Master FPD LINK chip meets the requirement [Ref(6)]  Confirm the local node and remote video master clock settings are matched |  |  |
| **CSI-2 /Parallel/Analog Interface**  Table [6] in DL\_FPD LINK III\_LINK\_REQ\_\_3.3.1.1    Confirm CSI-2 meets the interface specifications in the chipsets datasheets  Confirm the registers select the correcthardware inteface  Provide the evidence of the CSI-2 configuration set-up |  |  |

Table (4)

## 2.2 FPD LINK System Power up

|  |  |  |
| --- | --- | --- |
| **FPD LINK Checklist Items** | **Checklist items Evidence** | **Pass/ Fail/Comments** |
| **Auto configuration via pin strapping**  PL\_FPDLINK\_04\_005  **C**onfirm the hardware Pin strapping meets the requirements Ref[1]  Confirm the evidence in the Physical Layer Hardware DV |  |  |
| **I2C clock stretching**  DL\_FPD LINK\_REQ\_\_3.3.1.6  Confirm the Local and Remote nodes supports I2C clock streching and meets the specification Ref[6] |  |  |
| **Auto equalization behavior**  DL\_FPD LINK III\_LINK\_REQ\_\_3.3.2.1  Confirm chipset arrives in a stable lock condition as per requirement Ref[6] after reset  Show the evidence by scope plots or software simulation results |  |  |
| **FPD LINK Network Discovery at EOL/Service Bay**  DL\_FPD LINK\_REQ\_\_3.4.1.1  Confirm the local node and/or remote node sets apprioriate DTC for the configuration errors detected  Show the evidence by the software simulation results |  |  |
| **FPD LINK Network Errors and Reporting**  DL\_FPD LINK\_REQ\_\_3.4.2.1  DL\_FPD LINK\_REQ\_\_3.4.3.1  Confirm the each of the DTC’s, DID counters and the specific errors are set and reported by the CAN network  Confirm the evidence is shown in the Ref[6] |  |  |

Table (5)

# 2.3 Change Log

Record all changes made to this document in table (6)

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| --- | --- | --- |
| **Date** | **Changes made by**  **(Name and CDSID)** | **Changes made** |
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**Table (6)**